Keynote of Prof dr Wolfgang Ecker

Title:

How to Circumvent a RISCV Dead End

Speaker:

Wolfgang Ecker

Abstract:

RISCV is on everyone's lips: Politicians, researchers and product engineers as well as marketing are talking about RISCV. Many funded projects around RISCV are running, products are being developed and sold, and RISCV events and RISCV International – the owner of RISCV - are gaining attraction. RISCV is celebrated as an open alternative to proprietary ARM cores. Comparisons with Linux competing with Windows are made. In addition, RISCV offers to homogenize a wide set of cores inhouse developed at semiconductor companies and system houses.

The situation is reminiscent of VHDL about 40 years ago. A single HDL to describe digital hardware and the first language supported by RTL synthesis. May conferences were popping up all over the world and all CAD and design conferences had VHDL tracks. From today's point of view, VHDL is in a dead end, even though it is in use and slight improvements are being made.

This talk recapitulates the development of VHDL, compares the development paths of VHDL and RISCV and proposes a strategy to let RISCV avoid the VHDL fate: RISCV must go beyond RISCV.

CV: Wolfgang Ecker

Wolfgang Ecker is Distinguished Engineer at Infineon and Professor at Technical University of Munich. His research and innovation focus lie on digital system modeling, digital design automation, SoC architectures, embedded AI and AI for design automation.

Wolfgang Ecker published over 200 papers, received six publication awards and has been granted with the German EDA achievement award. He is member of Acatech, the German Academy of Science and Engineering and has been member of the AI commission of inquiry of the German Government.

Photo: Wolfgang Ecker